IN THE CLAIMS:

1. (Previously Amended) A semiconductor device comprising:

a lightly doped semiconductor substrate of a first conduction type;

a buried semiconductor layer of a second conduction type formed in a first region of the semiconductor substrate, spaced from a surface of the semiconductor substrate;

a semiconductor region of the second conduction type extending from the surface of the semiconductor substrate to a peripheral portion of the buried semiconductor layer, the semiconductor region of the second conduction type being connected to the buried semiconductor layer; and

a semiconductor region of the first conduction type formed in the semiconductor substrate surrounded by the buried semiconductor layer and the semiconductor region of the second conduction type, the semiconductor region of the first conduction type being isolated from the semiconductor substrate by the buried semiconductor layer and the semiconductor region of the second conduction type,

wherein a concentration of an impurity in the semiconductor region of the first conduction type is equal to a concentration of an impurity in the semiconductor substrate.

2. (Original) A semiconductor device according to claim 1, further comprising:

a first semiconductor element formed in the first conduction type region; and

a second semiconductor type semiconductor region being connected to a first potential,

the second region of the semiconductor substrate being connected to a second potential different from the first potential.

3. (Original) A semiconductor device according to claim 2, wherein

the second conduction type semiconductor region is extended over a third region adjacent to the first region of the semiconductor substrate;

the semiconductor device further comprises a third semiconductor element formed in the third region of the second conduction type semiconductor region; and

the second conduction type semiconductor region is connected to a third potential different at least the first potential or the second potential.

4. (Original) A semiconductor device according to claim 3, further comprising:

a well of the first conduction type formed in a fourth region in the third region; and

a fourth semiconductor element formed in the first conduction type well, and

the first conduction type well being connected to a fourth potential different from at least the first potential.

5. (Previously Amended) A semiconductor device according to claim 2, wherein

at least one of the first semiconductor element and the second semiconductor element is a memory cell.

6. (Previously Amended) A semiconductor device according to claim 3, wherein

at least one of the first semiconductor element and the second semiconductor element is a memory cell.

7. (Previously Amended) A semiconductor device according to claim 4, wherein

at least one of the first semiconductor element and the second semiconductor element is a memory cell.

8-22. (Canceled)